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IN THE SPECIFICATION

Please amend the paragraph starting on page 3, line 3 as follows:

Referring to FIG. 2, a circuit 20 is shown illustrating a conventional boundary scan connection with the boundary scan cells 22a-22n outside the I/O cells 24a-24n. Trying to connect the boundary scan cells 22a-22n, which are scattered over the entire die, can cause timing problems. Since the boundary scan flip flops are ~~connect~~ connected in a chain, routing issues cause severe hold time violations, thereby causing the chain to fail. However, placing the boundary scan cells 22a-22n manually is very time consuming (there typically exist hundreds of cells in a single device). For example, the manual placement process can take a number of days in a standard size design. Additionally, there is a clock tree at the top level to clock the boundary scan flip flops. Therefore, managing a reasonable skew at chip level is challenging, time consuming and area consuming. Furthermore, since more I/O cells are continually being added inside the I/O devices, timing modeling of the I/O devices need to be constantly updated.

Please amend the paragraph starting on page 16, line 3 as follows:

Referring to FIG. 9, a flip flop circuit 550 is shown. The flip flop circuit 550 may be implemented in the boundary scan

cells 304-310. However, the conventional boundary scan cells 22 may also benefit from the implementation of the flip flop circuit 550. The circuit 550 may be implemented without the inverter 502. The flip flop circuit 554 may provide significant power savings since the inverter 502 is removed. The setup time of the flip flop circuit 550 may be reduced by removing the delay through the inverter 502. The flip flop circuit 550 may have an area savings (e.g., the area of the inverter 502). The area needed for an additional gate 504 (e.g., a NAND gate) may be compensated by the area saved from the input inverter 502. The flip flop circuit 550 may have improved performance and have a power savings when compared with the circuit of FIG. 8. The flip flop circuit 550 may reduce crosstalk and noise impact of the scan connection (through reduction of the load at the data output, and reduction of the setup time through the removal of the decoupling inverter). The flip flop circuit 550 may also provide reduction of the switching capacitance on the clock tree (in a conventional circuit such as the circuit 20) and reduction of the switching load at the output of the flip flop, since the entire scan chain is ~~quite~~ quiet during the functional mode.